November 2000

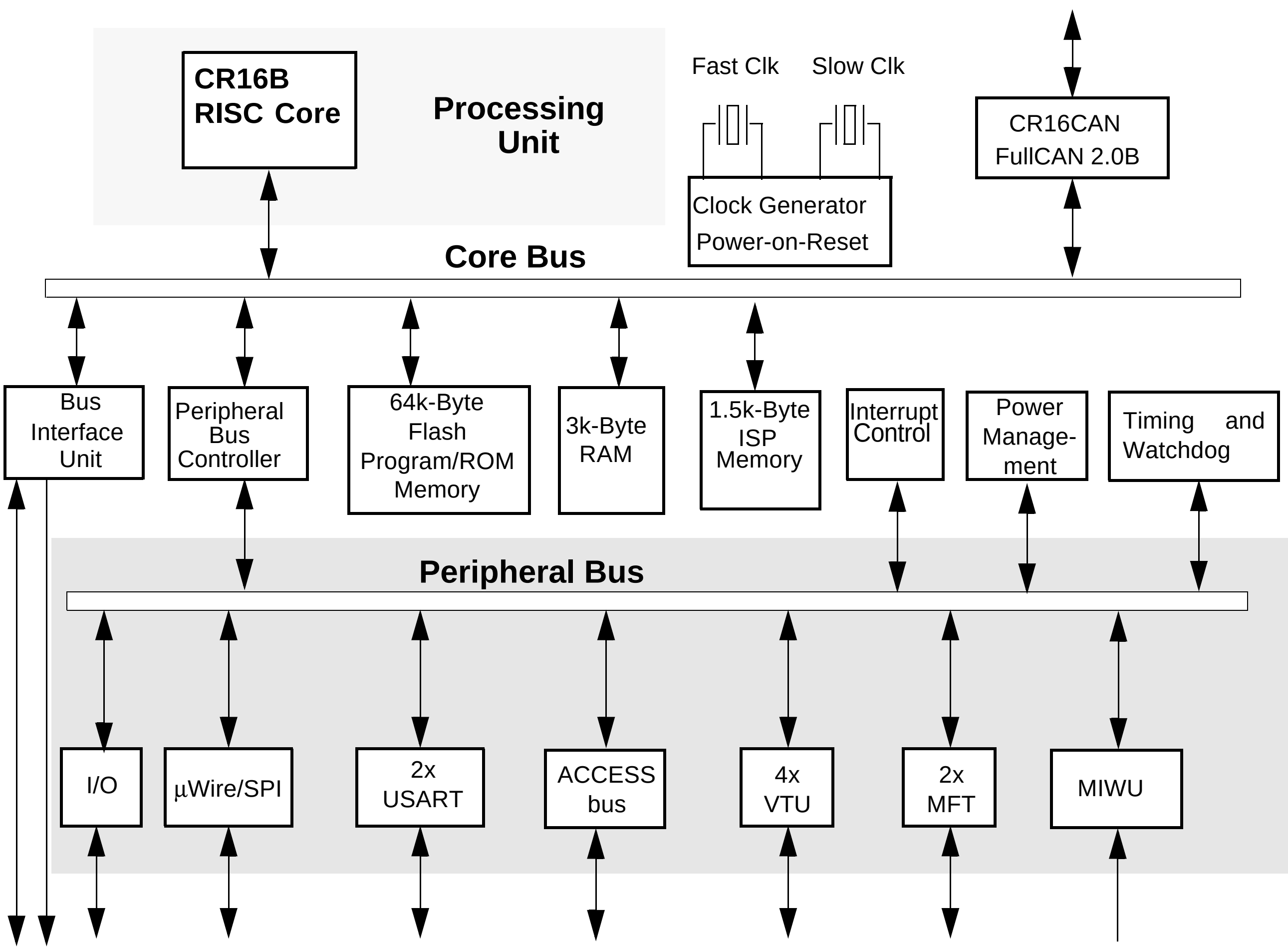
CR16MAS9/CR16MAS5 CompactRISC 16-Bit Reprogrammable/ROM Microcontroller

1.0 General Description

The CR16MAS9 and CR16MAS5 CompactRISC™ microcontroller is a general-purpose 16-bit microcontroller based on a Reduced Instruction Set Computer (RISC) architecture. The device operates as a complete microcomputer with all system timing, interrupt logic, flash program memory or ROM memory, RAM, and I/O ports included on-chip. It is ideally suited to a wide range of embedded controller applications because of its high performance, on-chip integrated features and low power consumption resulting in decreased system cost.

The CR16MAS9 and CR16MAS5 offer the high performance of a RISC architecture while retaining the advantages of a traditional Complex Instruction Set Computer (CISC): compact code, on-chip memory and I/O, and reduced cost. The CPU uses a three-stage instruction pipeline that allows execution of up to one instruction per clock cycle, or up to 25 million instructions per second (MIPS) at a clock rate of 25 MHz.

The CR16MAS9 and CR16MAS5 device contains a FullCAN class, CAN serial interface for low/high speed applications with 15 orthogonal message buffers, each supporting standard as well as extended message identifiers.



Note: Not all peripherals shown above will be contained in every device.

1.0 General Description (Continued)

The CR16MAS9 device has 64K bytes of reprogrammable flash EEPROM program memory or ROM memory, 1.5K bytes of flash EEPROM In-System-Programming memory, 3K bytes of static RAM, two USARTs, two 16-bit multi-function timers, one SPI/MICROWIRE-PLUS™ serial interface, WATCHDOG™ protection mechanism, and up to 56 general-purpose I/O pins.

The CR16MAS9 and CR16MAS5 devices operate with a high-frequency crystal as the main clock source and either the prescaled main clock source or with a low frequency (32.768 kHz) oscillator in Power Save mode. The device supports several Power Save modes which are combined with multi-source interrupt and wake-up capabilities.

This device also has a Versatile Timer Unit (VTU) with four timer sub-systems, a CAN interface, and ACCESS.bus synchronous serial bus interface.

Powerful cross-development tools are available from National Semiconductor and third party suppliers to support the development and debugging of application software for the CR16MAS9 and CR16MAS5. These tools let you program the application software in C and are designed to take full advantage of the CompactRISC architecture.

2.0 Features

- CPU Features
  - — Fully static core, capable of operating at any rate from 0 to 25 MHz (4 MHz minimum in active mode)
  - — 40 ns instruction cycle time with a 20 MHz external clock frequency
  - — Multi-source vectored interrupts (internal, external, and on-chip peripheral)
  - — Dual clock and reset
- On-chip power-on reset
- On-Chip Memory
  - — 64K bytes flash EEPROM program memory or ROM memory
  - — 3K bytes of static RAM data memory
  - — For flash program memory, 1.5k bytes flash EEPROM memory is used to store boot loader code
- On-Chip Peripherals
  - — Two Universal Synchronous/Asynchronous Receiver/Transmitter (USART) devices
  - — Two dual 16-bit multi-function timers (MFT1 and MFT2)
  - — 8/16-bit SPI/MICROWIRE-PLUS serial interface
  - — ACCESS.bus synchronous serial bus
  - — FullCAN interface with 15 message buffers complaint to CAN specification 2.0B active
  - — Versatile Timer Unit with four subsystems (VTU)
  - — Integrated WATCHDOG logic
- I/O Features
  - — Up to 56 general-purpose I/O pins (shared with on-chip peripheral I/O pins)
  - — Programmable I/O pin characteristics: TRI-STATE output, push-pull output, weak pull-up input, high-impedance input
  - — Schmitt triggers on general purpose inputs
- Power Supply
  - — 4.5V to 5.5V single-supply operation
- Temperature Range
  - — –40°C to +85°C
  - — –40°C to +125°C
- Development Support
  - — Real-time emulation and full program debug capabilities available
  - — CompactRISC tools provide C programming and debugging support

CR16 CompactRISC Microcontroller with CAN Interface Family Selection Guide

Programmable devices

NSID	Speed (MHz)	Flash (kByte)	EEPROM Data Memory (Bytes)	SRAM (kBytes)	USART	Timer	I/Os	Temp. Range	Peripherals	Package Type
CR16MAS9VJEx	25	64		3	2	2MFT VTU	56	E, I	CAN,	80PQFP

ROM devices

NSID	Speed (MHz)	ROM (KByte)	EEPROM Data Memory (Bytes)	SRAM (kBytes)	USART	Timer	I/Os	Temp. Range	Peripherals	Package Type
CR16MAS5VJExy	25	64		3	2	2MFT VTU	56	E, I	CAN	80PQFP

Note:

- Suffix x in the NSID is defined below:

Temperature Ranges:

I = Industrial	-40°C to +85°C is represented when x is 8
E = Extended	-40°C to +125°C is represented when x is 7

- Suffix y in the NSID defines the ROM code.

Note: All devices contains Access.bus (ACB), Clock and Reset, MICROWIRE/API, Multi-Input Wake-Up (MIWU), Power Management (PMM), and the Real-Time Timer and Watchdog (TWM) modules. Access.bus is compatible with I2C bus offered by Philips Semiconductor.

CR16 CompactRISC Microcontroller with CAN Interface Family Devices

National Semiconductor currently offers a variety of the CR16 CompactRISC Microcontrollers with CAN interface. The CR16MAS offer complete functionality in an 80-pin PQFP package.

3.0 Device Overview

The CR16MAS9 and CR16MAS5 CompactRISC microcontroller are complete microcomputers with all system timing, interrupt logic, program memory, data memory, and I/O ports included on-chip, making it well-suited to a wide range of embedded controller applications. The block diagram on page 1 of the data sheet shows the major on-chip components of the CR16MAS9.

3.1 CR16B CPU CORE

The CR16MAS9 and CR16MAS5 uses the CR16B CPU core module. This is the same core used in other CompactRISC family member designs, like DECT or GSM chipsets.

The high performance of the CPU core results from the implementation of a pipelined architecture with a two-bytes-per-cycle pipelined system bus. As a result, the CPU can support a peak execution rate of one instruction per clock cycle.

Compared with conventional RISC processors, the CR16MAS9 and CR16MAS5 differ in the following ways:

— The CPU core can use on-chip rather than external memory. This eliminates the need for large and complex bus interface units.

— Most instructions are 16 bits, so all basic instructions are just two bytes long. Additional bytes are sometimes required for immediate values, so instructions can be two or four bytes long.

— Non-aligned word access is allowed. Each instruction can operate on 8-bit or 16-bit data.

— The device is designed to operate with a clock rate in the 10 to 25 MHz range rather than 100 MHz or more. Most embedded systems face EMI and noise constraints that limit clock speed to these lower ranges. A lower clock speed means a simpler, less costly silicon implementation.

— The instruction pipeline uses three stages. A smaller pipeline eliminates the need for costly branch prediction mechanisms and bypass registers, while maintaining adequate performance for typical embedded controller applications.

For more information, please refer to the CR16B Programmer's Reference Manual, Literature #: 633150.

3.2 MEMORY

The CompactRISC architecture supports a uniform linear address space of 2 megabytes. The CR16MAS9 and CR16MAS5 implementation of this architecture uses only the lowest 128K bytes of address space. Three types of on-chip memory occupy specific intervals within this address space:

- 64K bytes of flash EEPROM program memory or ROM memory
- 3K bytes of static RAM
- 1.5K bytes flash EEPROM memory for ISP code

The 3K bytes of static RAM are used for temporary storage of data and for the program stack and interrupt stack. Read and write operations can be byte-wide or word-wide, depending on the instruction executed by the CPU. Each memory access requires one clock cycle; no wait cycles or hold cycles are required.

The 64K bytes of flash EEPROM program memory are used to store the application program. It has security features to prevent unintentional programming and to prevent unauthorized access to the program code. This memory can be programmed with a CR16MAS9 external programming unit or with the CR16MAS9 installed in the application system (in-system programming).

There is a factory programmed boot memory used to store In-System-Programming (ISP) code. (This code allows programming of the program memory via one of the USART interfaces in the final application.)

For flash EEPROM program memory, the device internally generates the necessary voltages for programming. No additional power supply is required.

3.3 INPUT/OUTPUT PORTS

The CR16MAS9 and CR16MAS5 devices have 56 software-configurable I/O pins, organized into seven 8-pin ports called Port B, Port C, Port F, Port G, Port H, Port I, and Port L. Each pin can be configured to operate as a general-purpose input or general-purpose output. In addition, many I/O pins can be configured to operate as a designated input or output for an on-chip peripheral module such as the USART, timer, or MICROWIRE/SPI interface.

The I/O pin characteristics are fully programmable. Each pin can be configured to operate as a TRI-STATE output, push-pull output, weak pull-up input, or high-impedance input.

3.4 BUS INTERFACE UNIT

The Bus Interface Unit (BIU) controls the interface between the on-chip modules to the internal core bus. It determines the configured parameters for bus access (such as the number of wait states for memory access) and issues the appropriate bus signals for each requested access.

The BIU uses a set of control registers to determine how many wait states and hold states are to be used when accessing flash EEPROM program memory, ISP memory and the I/O area (Port B and Port C). Upon start-up the configuration registers are set for slowest possible memory access. To achieve fastest possible program execution, appropriate values should be programmed. These settings vary with the clock frequency and the type of on-chip device being accessed.

3.5 INTERRUPTS

The Interrupt Control Unit (ICU31L) receives interrupt requests from internal and external sources and generates interrupts to the CPU. An interrupt is an event that temporarily stops the normal flow of program/ROM execution and causes a separate interrupt service routine to be executed. After the interrupt is serviced, CPU execution continues with the next instruction in the program following the point of interruption.

Interrupts from the timers, USARTs, MICROWIRE/SPI interface, multi-input wake-up, and A/D converter are all maskable interrupts; they can be enabled or disabled by the software. There are 32 of these maskable interrupts, organized into 32 predetermined levels of priority.

The highest-priority interrupt is the Non-Maskable Interrupt ($\overline{NMI}$), which is generated by a signal received on the $\overline{NMI}$ input pin.

3.6 MULTI-INPUT WAKE-UP

The Multi-Input Wake-Up (MIWU16) module can be used for either of two purposes: to provide inputs for waking up (exiting) from the HALT, IDLE, or Power Save mode; or to provide general-purpose edge-triggered maskable interrupts from external sources. This 16-channel module generates four programmable interrupts to the CPU based on the signals received on its 16 input channels. Channels can be individually enabled or disabled, and programmed to respond to positive or negative edges.

3.7 DUAL CLOCK AND RESET

The Dual Clock and Reset (CLK2RES) module generates a high-speed main system clock from an external crystal network. It also provides the main system reset signal and a power-on reset function.

This module also generates a slow system clock (32.768 kHz) from another external crystal network. The slow clock is used for operating the device in power-save mode. Without a 32.768kHz external crystal network, the low speed system clock can be derived from the high speed clock by a prescaler.

Also, two independent clocks divided down from the high speed clock are available on output pins.

3.8 POWER MANAGEMENT

The Power Management Module (PMM) improves the efficiency of the CR16MAS9 and CR16MAS5 devices by changing the operating mode and therefore the power consumption according to the required level of activity.

The CR16MAS9 and CR16MAS5 devices can operate in any of four power modes:

- Active: The device operates at full speed using the high-frequency clock. All device functions are fully operational.
- Power Save: The device operates at reduced speed using the slow clock. The CPU and some modules can continue to operate at this low speed.
- IDLE: The device is inactive except for the Power Management Module and Timing and Watchdog Module, which continue to operate using the slow clock.
- HALT: The device is inactive but still retains its internal state (RAM and register contents).

3.9 MULTI-FUNCTION TIMER

The Multi-Function Timer (MFT16) module contains two independent timer/counter units called MFT1 and MFT2, each containing a pair of 16-bit timer/counter registers. Each timer/counter unit can be configured to operate in any of the following modes:

- Processor-Independent Pulse Width Modulation (PWM) mode, which generates pulses of a specified width and duty cycle, and which also provides a general-purpose timer/counter.
- Dual Input Capture mode, which measures the elapsed time between occurrences of external events, and which also provides a general-purpose timer/counter.
- Dual Independent Timer mode, which generates system timing signals or counts occurrences of external events.
- Single Input Capture and Single Timer mode, which provides one external event counter and one system timer.

3.10 VERSATILE TIMER UNIT

The Versatile Timer Unit (VTU) module contains four independent timer subsystems, each operating in either dual 8-bit PWM configuration, as a single 16-bit PWM timer, or a 16-bit counter with two input capture channels. Each of the four timer subsystems offer an 8-bit clock prescaler to accommodate a wide range of frequencies.

3.11 REAL-TIME TIMER AND WATCHDOG

The Timing and Watchdog Module (TWM) generates the clocks and interrupts used for timing periodic functions in the system. It also provides Watchdog protection against software errors. The module operates on the slow system clock.

The real-time timer can generate a periodic interrupt to the CPU at a software-programmed interval. This can be used for real-time functions such as a time-of-day clock. The real-time timer can trigger a wake-up condition from power-save mode via the Multi-Input Wake-Up module.

The Watchdog is designed to detect program execution errors such as an infinite loop or a “runaway” program. Once Watchdog operation is initiated, the application program must periodically write a specific value to a Watchdog register, within specific time intervals. If the software fails to do so, a Watchdog error is triggered, which resets the device.

3.12 USART

The USART supports a wide range of programmable baud rates and data formats, and handles parity generation and several error detection schemes. The baud rate is generated on-chip, under software control.

There are two independent USARTs in the CR16MAS9 and CR16MAS5 devices and they offer a wake-up condition from the power-save mode via the Multi-Input Wake-Up module.

3.13 MICROWIRE/SPI

The MICROWIRE/SPI (MWSPI) interface module supports synchronous serial communications with other devices that conform to MICROWIRE or Serial Peripheral Interface (SPI) specifications. It supports 8-bit and 16-bit data transfers.

The MICROWIRE interface allows several devices to communicate over a single system consisting of four wires: serial in, serial out, shift clock, and slave enable. At any given time, the MICROWIRE interface operates as the master or a slave. The CR16MAS9 and CR16MAS5 support the full set of slave select for multi-slave implementation.

In master mode, the shift clock is generated on chip under software control. In slave mode, a wake-up out of power-save mode is triggered via the Multi-Input Wake-Up module.

3.14 CR16CAN

The CR16CAN device contains a FullCAN class, CAN serial bus interface for applications that require a high speed (up to 1MBits per second) or a low speed interface with CAN bus master capability. The data transfer between CAN and the CPU is established by 15 memory mapped message buffers, which can be individually configured as receive or transmit buffers. An incoming message is filtered by two masks, one for the first 14 message buffers and another one for the 15th message buffer to provide a basic CAN path. A priority decoder allows any buffer to have the highest or lowest transmit priority. Remote transmission requests can be processed automatically by automatic reconfiguration to a receiver after transmission or by automated transmit scheduling upon reception. In addition, a time stamp counter (16-bits wide) is provided to support real time applications.

The CR16CAN device is a fast core bus peripheral, which allows single cycle byte or word read/write access. A set of diagnostic features (such as loopback, listen only, and error identification) support the development with the CR16CAN module and provide a sophisticated error management tool.

The CR16CAN receiver can trigger a wake-up condition out of the power-save modes via the Multi-Input Wake-Up module.

3.15 ACCESS.BUS INTERFACE

The ACCESS.bus interface module (ACB) is a two-wire serial interface with the ACCESS.bus physical layer. It is also compatible with Intel's System Management Bus (SMBus) and Philips' I^2C bus. The ACB module can be configured as a bus master or slave, and can maintain bi-directional communications with both multiple master and slave devices.

The ACCESS.bus receiver can trigger a wake-up condition out of the power-save modes via the Multi-Input Wake-Up module.

3.16 DEVELOPMENT SUPPORT

A powerful cross-development tool set is available from National Semiconductor and third parties to support the development and debugging of application software for the CR16MAS9 and CR16MAS5. The tool set lets you program the application software in C and is designed to take full advantage of the CompactRISC architecture.

There are In-System Emulation (ISE) devices available for the CR16MAS9 and CR16MAS5 from iSYSTEM™, as well as lower-cost evaluation boards. See your National Semiconductor sales representative for current information on availability and features of emulation equipment and evaluation boards.

4.0 Memory Map

The CompactRISC architecture supports a uniform linear address space of 2 megabytes. The device implementation of this architecture uses only the lowest 128K bytes of address space, ranging from 0000 to 1FFFF hex. Table 1 is a memory map showing the types of memory and peripherals that occupy this memory space. Address ranges not listed in the table are reserved and should not be read or written.

Table 1 Device Memory Map

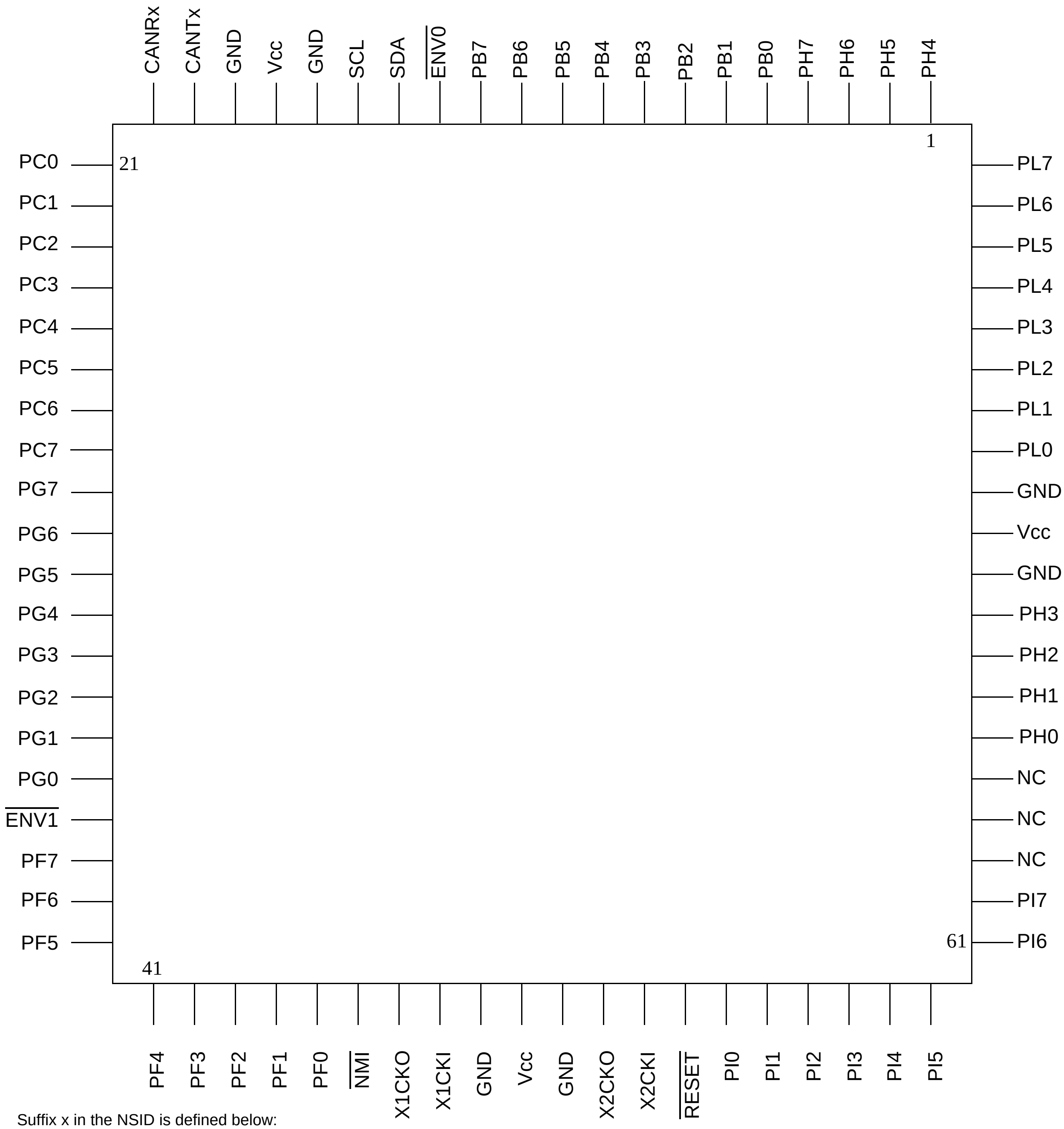
Address Range (hex)	Description
0000-BFFF	Flash/ROM Program Memory
C000-CBFF	Static RAM (3K bytes)
E000-E5FF	ISP Memory(1.5K bytes)
F400-F7FF	CAN buffers and registers (1K bytes)
F800-FAFF	BIU Peripherals (768 bytes)
FB00-FB06	Port B registers
FB00-FBFF	I/O Expansion + Ports PB & PC (256 bytes)
FB10-FB16	Port C registers
FC00-FFFF	Peripherals and other I/O Ports (1K bytes)
FC40-FC8A	Clock, Power Management, and Wake-Up registers
FCA0-FCA8	Port G registers
FCC0-FCC8	Port H registers
FF00-FF08	Port L registers
FD20-FD28	Port F registers
FE00-FE1E	Interrupt Control Unit registers
FE40-FE4E	USART 1 registers
FE60-FE66	MICROWIRE registers
FE80-FE8E	USART 2 registers
FEC0-FECA	ACCESS.bus registers
FEE0-FEE8	Port I registers
FF20-FF2A	Timer and WATCHDOG registers
FF40-FF50	Multi-function Timer1 registers
FF60-FF70	Multi-function Timer2 registers
FF80-FFA4	Versatile Timer Unit registers
1C000-1FFFF	Flash Program Memory (16K bytes)[a]

[a]. Not available on ROM devices

5.0 Device Pinouts

The CR16MAS9 and CR16MAS5 are available in the 80-pin PQFP package.

Figure 1 shows the pin assignments for this package.



- Suffix x in the NSID is defined below:

  Temperature Ranges:

  x = 7 is -40°C to +125°C
  = 8 is -40°C to +85°C

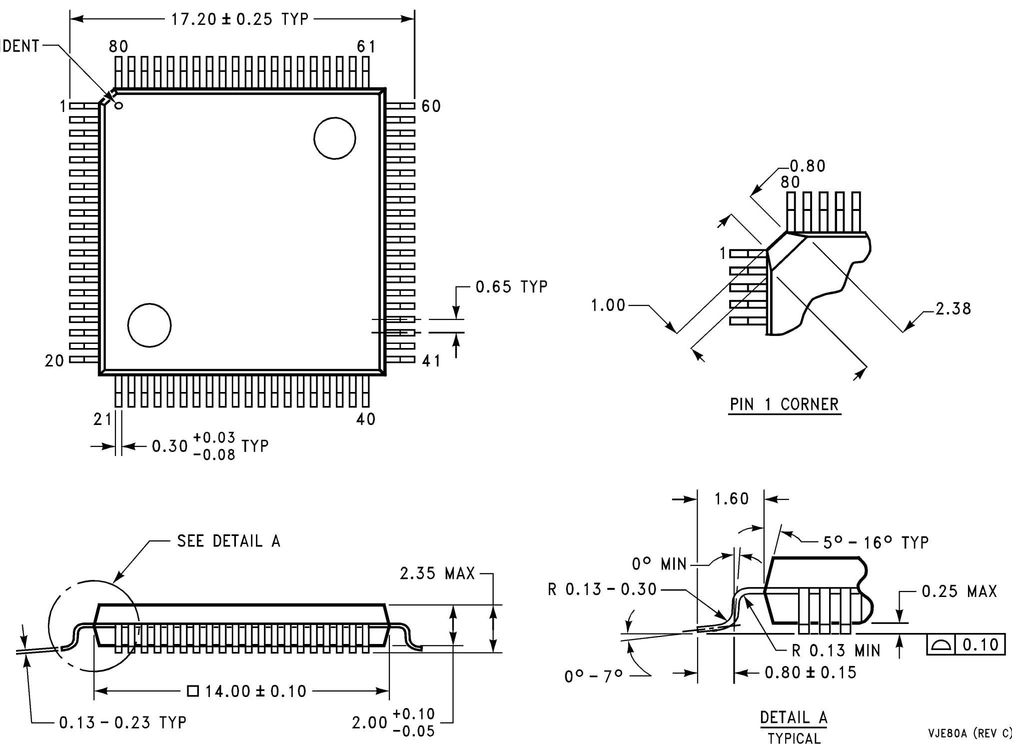
- Suffix y in the NSID defines the ROM code.

Top View

Order Number CR16MAS9VJEx or CR16MAS5VJExy
See NS Package Number VJE80A

Figure 1. 80-Pin PQFP Package Connection Diagram

6.0 Physical Dimensions inches (millimeters) unless otherwise noted



80 Lead Molded Plastic Quad Flat Package
Order Number CR16MAS9VJEx or CR16MAS5VJExy
See NS Package Number VJE80A

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